UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/929,047	08/15/2001	Makoto Suwada	1341.1104	9906

21171   7590   01/13/2005

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EXAMINER
STEVENS, THOMAS H

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/929,047	SUWADA ET AL.
	Examin r	Art Unit
	Thomas H. Stevens	2123

-- *The MAILING DATE of this communication appears on the cov r sh t with the corr spondence addr ss --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _15 August 2001_.

2a)☐ This action is FINAL.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-9_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-9_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _15 August 2001_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☒ Certified copies of the priority documents have been received in Application No. _2000-273268_.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _8/14/01_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-9 have been examined.

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and
> process of making and using it, in such full, clear, concise, and exact terms as to enable any
> person skilled in the art to which it pertains, or with which it is most nearly connected, to make
> and use the same and shall set forth the best mode contemplated by the inventor of carrying
> out his invention.

3.   Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claims contains subject

matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventors, at the time

the application was filed, had possession of the claimed invention. The

specification's definition of " preset threshold" is unclear as to whether the

software or the purchaser is creating the value.

Claim Rejections - 35 USC § 103

4.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1,

148 USPQ 459 (1966), that are applied for establishing a background for

determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

        1.   Determining the scope and contents of the prior art.

        2.   Ascertaining the differences between the prior art and the claims at

                issue.

        3.   Resolving the level of ordinary skill in the pertinent art.

       4.   Considering objective evidence present in the application indicating

obviousness or nonobviousness.

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable

Srivastava et al., ("Symbolic Approximation of Analog Circuits Using Sspice;

IEEE (1990)) in view of Nabors et al. (U.S. 6,088,523 (2000)). Srivastava et al.

teaches a Spice circuit analyzer and approximator, with a user-selected

threshold, for AC analysis of for active devices; but doesn't cover pass circuits.

Nabors et al., teaches a method and apparatus for making electrical (passive)

circuits (abstract).

At the time of invention, it would have been obvious to one of ordinary skill in the

art to modify Nabors et al by way of Srivastava et al to encompass passive and

active circuit analysis.

Claim 1. A high-frequency-corresponding simulation (Nabors: column 2, lines21-

25; lines 33-41;and Srivastava: pg. 509, Sspice Element Definitions) apparatus

comprising: an element setting unit which sets plurality of elements

corresponding to wiring patterns (Nabors: column 1, lines 52-65;column 2, lines

33-41) in accordance with circuit design information; a resistance-value

calculation unit which calculates the total of resistance values each of which is

the sum of the DC resistance (low frequencies: Nabors: columns 1-2, lines 65-67

and 1-5) value and of the elements as the total skin resistance (Nabors: column

16, lines 3-15) value of each resistance value; a first determination unit which

determines whether the total resistance (Nabors: column 3, lines 60-67) value is

less than a first threshold value (Srivastava: pg. 510, lines 22-26); a sorting unit

which sorts resistance values corresponding to the elements when the total

resistance value (Nabors: column 3, lines 60-67 to column 4, lines 1-15) equal to

or larger than the first threshold value (Srivastava: pg. 510, lines 22-26) in

accordance with determination result said first determination unit (Nabor: column

5, lines 22-40); a second determination unit which integrates the resistance

values starting with a resistance value having the smallest high-frequency

element delay (Nabors: column 7, lines 6-8) and determines whether the   .

integration result reaches before a second threshold (Srivastava: pg. 510, lines

22-26) value whenever is executed; and an analysis unit which executes an

analysis by using an element corresponding to an integrated resistance value as

a RLC model and elements (examiner assumes this section of claim details new

equivalent circuit: Nabors: column 8, lines 19-25) other than the element as high-

frequency element models when determination unit determines said second that

the integration result reaches the value immediately before the second threshold

value (Srivastava: pg. 510, lines 22-26).

Claim 2. The high-frequency-corresponding simulation apparatus according to

claim 1, (Nabors: column 2, lines21-25; lines 33-41;and Srivastava: pg. 509,

Sspice Element Definitions) wherein said analysis unit executes an analysis by

using all elements as RLC (examiner assumes this section of claim details new

equivalent circuit: Nabors: column 8, lines 19-25) models when the total

resistance value less than first threshold (Srivastava: pg. 510, lines 22-26) value.

Claim 3. The high-frequency-corresponding simulation apparatus according to

claim 1, (Nabors: column 2, lines21-25; lines 33-41;and Srivastava: pg. 509,

Sspice Element Definitions) wherein said analysis unit superimposes a skin

resistance (Nabors: column 16, lines 3-15) value on a DC resistance value a

RLC model.

Claim 4. The high-frequency-corresponding simulation apparatus according to

claim 1, (Nabors: column 2, lines21-25; lines 33-41;and Srivastava: pg. 509,

Sspice Element Definitions) further comprising a setting change unit, which

changes the value of the second threshold (Srivastava: pg. 510, lines 22-26)

value.

Claim 5. The high-frequency-corresponding simulation apparatus according to claim 4, (Nabors: column 2, lines21-25; lines 33-41;and Srivastava: pg. 509, Sspice Element Definitions; Srivastava: pg. 510, lines 22-26) wherein said setting change unit also changes the value of a skin resistance (Nabors: column 16, lines 3-15) value to be superimposed on the DC resistance value.

Claim 6. The high-frequency-corresponding simulation apparatus according to claim 1, (Nabors: column 2, lines21-25; lines 33-41;and Srivastava: pg. 509, Sspice Element Definitions; Srivastava: pg. 510, lines 22-26) wherein said circuit is constituted of a plurality substrates (Nabors: column 8, lines 55-62).

Claim 7. A high-frequency-corresponding simulation method (Nabors: column 2, lines21-25; lines 33-41;and Srivastava: pg. 509, Sspice Element Definitions; Srivastava: pg. 510, lines 22-26) comprising the steps of: setting plurality elements corresponding to in accordance with circuit design wiring patterns information (Nabors: column 1, lines 52-65;column 2, lines 33-41); calculating the total resistance values each of which is the sum of the DC resistance (low frequencies: Nabors: columns 1-2, lines 65-67 and 1-5) value and skin resistance value of each of the elements as the total resistance value (Nabors: column 3, lines 60-67); determining whether the total resistance value is less than a first threshold value (Srivastava: pg. 510, lines 22-26); the elements by using a high-frequency element delay as a key when it is determined that the total resistance (Nabors: column 3, lines 60-67) value equal to or larger than the first threshold

value (Srivastava: pg. 510, lines 22-26); integrating the resistance values starting

with resistance value having the smallest high-frequency element delay;

determining whether the result of integration reaches a value immediately before

a second threshold value (Srivastava: pg. 510, lines 22-26) whenever the

integration is executed; and executing an analysis by corresponding using an

element to an integrated resistance value as a RLC model and (examiner

assumes this section of claim details new equivalent circuit: Nabors: column 8,

lines 19-25) element models when other than the element as high-frequency is

determined that the integration result reaches the value immediately before

second threshold value (Srivastava: pg. 510, lines 22-26).

Claim 8. A computer-readable recording medium which stores computer program

which when executed on a computer realizes (Nabors: columns 17 and 18, lines

66-67 and 1-26, respectively; Srivastava: abstract) the steps of: setting plurality

of elements corresponding to wiring patterns accordance with circuit design

information; calculating the total of resistance values each of which is the sum of

the DC resistance (low frequencies: Nabors: columns 1-2, lines 65-67 and 1-5)

value and skin resistance (Nabors: column 16, lines 3-15) value of each of the

elements as the total resistance value (Nabors: column 3, lines 60-67);

determining whether the total resistance (Nabors: column 3, lines 60-67) value is

less than a first threshold value (Srivastava: pg. 510, lines 22-26); sorting

resistance values corresponding to the elements by using a high-frequency

element delay (Nabors: column 4, lines 55-61) as a key when it is determined

that the resistance value is equal to or larger than the first threshold value;

integrating the resistance values starting with a resistance value having the

smallest high-frequency element delay (Nabors: column 8, lines 50-62);

determining whether the result of integration reaches a value immediately before

a second threshold (Srivastava: pg. 510, lines 22-26) value whenever the

integration is executed; and executing an analysis by using an element

corresponding to an integrated resistance value as a RLC (examiner assumes

this section of claim details new equivalent circuit: Nabors: column 8, lines 19-25)

model and elements other than the element as high-frequency element models

when it is determined that the integration result reaches the value threshold value

(Srivastava: pg. 510, lines 22-26).

Claim 9. A computer program which when executed on a computer (Nabors:

columns 17 and 18, lines 66-67 and 1-26, respectively) realizes the steps of:

setting a plurality of elements corresponding to wiring patterns (Nabors: column

1, lines 52-65;column 2, lines 33-41) in accordance with circuit design

information; calculating the total of resistance values each of which is the sum of

the DC resistance (low frequencies: Nabors: columns 1-2, lines 65-67 and 1-5)

value and skin resistance (Nabors: column 16, lines 3-15) value of each of the

elements as the total resistance value (Nabors: column 3, lines 60-67);

determining whether the total resistance (Nabors: column 3, lines 60-67) value is

less than a first threshold value; sorting resistance values corresponding to the

elements by using a high-frequency element delay as a key when it determined

that the total resistance value is equal to or larger than the first threshold

(Srivastava: pg. 510, lines 22-26) value; integrating the resistance values starting

with a resistance value (Nabors: column 3, lines 60-67) having the smallest high-

frequency element delay; determining whether the result of integration reaches a

value immediately before a second threshold (Srivastava: pg. 510, lines 22-26)

value whenever the integration is executed; and executing an analysis by using

an element corresponding to an integrated resistance value as a RLC (examiner

assumes this section of claim details new equivalent circuit: Nabors: column 8,

lines 19-25) model and elements other than the element as high-frequency

element models when determined that the result reaches the value immediately

before integration second threshold value (Srivastava: pg. 510, lines 22-26).

Correspondence Information

Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Mr. Tom Stevens whose telephone number is

571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr.

Kevin Teska at (571) 272-3716. Fax number is 571-273-3715

Any inquires of general nature or relating to the status of this application

should be directed to the Group receptionist whose phone number is (571) 272-

1400

January 5, 2005

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER